OpenPOWER and Acceleration

Brad McCredie
VP, IBM Fellow
IBM Cognitive Systems Development

Jerry Chen
Industrial AI Business & Ecosystem Development
Nvidia

March 19, 2018
Fundamental forces are accelerating change in our industry

IT innovation can no longer come from just the processor

Moore’s Law

Full system stack innovation required

2000 2020

Firmware / OS
Accelerators
Software
Storage
Network

(Lower is better)

IT consumption models are expanding

Cognitive

Custom Hyperscale
Data Centers

Hybrid Cloud

Open Solutions

Not only is Moore’s Law “coming to an end in practical term, in that chip speeds can be expected to stall, but it is actually likely to roll back in terms of performance ...” - William Holt, Intel Executive Vice President and General Manager
Validation from a Legend...
Cognitive Solutions redefine our traditional IT market

Conservatively add 50% to our market by 2020 … likely much more

$860B +25% CAGR

$1,685B +5% CAGR

New Market Addressable by Cognitive Solutions

...and half of annual VC investment
Creating an Open Processor Ecosystem for POWER (OpenPOWER)

System Operating Environment Software Stack

A modern development environment is emerging based on tools and services

Power Open Source Software Stack Components

- Cloud Software
- Standard Operating Environment (System Mgmt)
- Operating System / KVM
- Firmware
- Hardware

Existing Open Source Software Communities

New OSS Community

Software

- OpenPOWER Firmware
- OpenPOWER Technology

Firmware

Hardware

Multiple Options to Design with POWER Technology Within OpenPOWER

- POWER8
- CAPI over PCIe

Framework to Integrate System IP on Chip

“Standard POWER Products” - 2014

40,000 packages now available

“Custom POWER SoC” - Future

Industry IP License Model
Acceleration Can Have a Bigger Impact on Cost/Performance than Processors

Multiple Options to Design with POWER Technology Within OpenPOWER

POWER8

CAPI over PCIe

“Standard POWER Products” - 2014

Framework to Integrate System IP on Chip

Customizable

“Custom POWER SoC” - Future

Industry IP License Model

OpenCAPI & NVLink

FPGA
GPU
Storage Class Memories
High-performance Networking
Other Stuff...
## Proposed POWER Processor Technology and I/O Roadmap

<table>
<thead>
<tr>
<th>Year</th>
<th>Model</th>
<th>Cores</th>
<th>Technology</th>
<th>Micro-Architecture</th>
<th>Process Technology</th>
<th>I/O Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td>POWER7</td>
<td>8</td>
<td>45nm</td>
<td>New Micro-Architecture</td>
<td>New Process Technology</td>
<td>Up To 65 GB/s</td>
</tr>
<tr>
<td>2012</td>
<td>POWER7+</td>
<td>8</td>
<td>32nm</td>
<td>Enhanced Micro-Architecture</td>
<td>New Process Technology</td>
<td>PCIe Gen2</td>
</tr>
<tr>
<td>2014</td>
<td>POWER8</td>
<td>12</td>
<td>22nm</td>
<td>New Micro-Architecture</td>
<td>New Process Technology</td>
<td>Up To 210 GB/s</td>
</tr>
<tr>
<td>2016</td>
<td>POWER8 w/ NVLink</td>
<td>12</td>
<td>14nm</td>
<td>Enhanced Micro-Architecture With NVLink</td>
<td>New Process Technology</td>
<td>PCIe Gen3</td>
</tr>
<tr>
<td>2017</td>
<td>P9 SO</td>
<td>24</td>
<td>14nm</td>
<td>New Micro-Architecture</td>
<td>Direct attach memory</td>
<td>PCIe Gen4 x48</td>
</tr>
<tr>
<td>2018</td>
<td>P9 SU</td>
<td>24</td>
<td>14nm</td>
<td>Enhanced Micro-Architecture</td>
<td>Buffered Memory</td>
<td>PCIe Gen4 x48</td>
</tr>
<tr>
<td>2019</td>
<td>P9 w/ Adv. I/O</td>
<td>24</td>
<td>14nm</td>
<td>Enhanced Micro-Architecture</td>
<td>New Memory Subsystem</td>
<td>PCIe Gen5</td>
</tr>
</tbody>
</table>

### Sustained Memory Bandwidth
- **POWER7**: Up To 65 GB/s
- **POWER7+**: Up To 65 GB/s
- **POWER8**: Up To 210 GB/s
- **POWER8 w/ NVLink**: Up To 210 GB/s
- **P9 SO**: Up To 150 GB/s
- **P9 SU**: Up To 210 GB/s
- **P9 w/ Adv. I/O**: Up To 350 GB/s

### Standard I/O Interconnect
- **POWER7**: PCIe Gen2
- **POWER7+**: PCIe Gen2
- **POWER8**: PCIe Gen3
- **POWER8 w/ NVLink**: PCIe Gen3
- **P9 SO**: PCIe Gen4 x48
- **P9 SU**: PCIe Gen4 x48
- **P9 w/ Adv. I/O**: PCIe Gen5

### Advanced I/O Signaling
- **POWER7**: N/A
- **POWER7+**: N/A
- **POWER8**: N/A
- **POWER8 w/ NVLink**: 20 GT/s, 160GB/s
- **P9 SO**: 25 GT/s, 300GB/s
- **P9 SU**: 25 GT/s, 300GB/s
- **P9 w/ Adv. I/O**: 32 & 50 GT/s

### Advanced I/O Architecture
- **POWER7**: N/A
- **POWER7+**: N/A
- **POWER8**: CAPI 1.0
- **POWER8 w/ NVLink**: CAPI 1.0, NVLink 1.0
- **P9 SO**: CAPI 2.0, OpenCAPI3.0, NVLink2.0
- **P9 SU**: CAPI 2.0, OpenCAPI3.0, NVLink2.0
- **P9 w/ Adv. I/O**: CAPI 2.0, OpenCAPI4.0, NVLink

*Statement of Direction, Subject to Change*
Future Evolution of System Architecture

Yesterday’s Plumbing
Tomorrow’s Differentiation

OpenCAPI Northbound

Cores & Caches

System Bus
768 GB/s

Cores & Caches

Cores & Caches

JEDEC Buffer

OpenCAPI & PCI

Yesterday’s Plumbing
Tomorrow’s Differentiation

PCI Gen X

OpenCAPI / NVLink

CPU/Accelerator Bandwidth

CPU
1x

Accelerator

GPU

CPU
2x

Accelerator

GPU

NVIDIA GPU
5x

Accelerator
7-10x

System bottleneck