OpenPOWER
Moving on from Moore’s Law
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Today’s Talk

Part I: Slowdown of Moore’s Law - The Supply-Demand Gap
Part II: OpenPOWER - Core and System Innovations
Technology Trends

Based on SPECintCPU. Source: John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e. 2018
Growing Demand

1 Billion Users

fueling exponential growth in data
Growing Demand

1 Billion Users

fueling exponential growth in data
More Cores & Threads

- More Cores
- More Threads

Memory Hierarchy for Websearch HPCA 2018  Source: Grant Ayers, Jung Ho Ahn, Christos Kozyrakis, Parthasarathy Ranganthan
More Memory Bandwidth

**Kelp QoS for Accelerated ML Systems - ISCA 2018 Submission**

Source: Haishan Zhu, David Low

**DRAM Bandwidth Contention Impacts RNN server execution**
## More Memory

<table>
<thead>
<tr>
<th></th>
<th>DRAM (DDR4)</th>
<th>Big Gap</th>
<th>Flash (NAND)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface</td>
<td>64B L/S</td>
<td>⇐ 1000X better lat</td>
<td>4KiB block PCIe</td>
</tr>
<tr>
<td>GiB/Device</td>
<td>16 / 32</td>
<td>⇐ 30X better BW</td>
<td>~3000 usable</td>
</tr>
<tr>
<td>$/GiB</td>
<td>100% of DRAM</td>
<td>⇐ Load/store</td>
<td>~10% of DRAM</td>
</tr>
<tr>
<td>Latency</td>
<td>85/150 ns (NUMA local/remote)</td>
<td>0(10X) more GB ⇒ 10X better $/GB ⇒ Persistent ⇒</td>
<td>100 us (500 us 99% tail)</td>
</tr>
<tr>
<td>Channel bandwidth</td>
<td>~16 GB/s Read (sequential)</td>
<td></td>
<td>6 GB/s Read (64KB blk)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4 GB/s Write (64KB blk)</td>
</tr>
</tbody>
</table>

Optionality and Open System Solutions: OpenCAPI NVM, Samsung ZSSD, Intel Optane

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2017 ISCA Keynote More Moor - Source: Parthasarathy Ranganthan
Zaius

Dual socket P9 LaGrange CPU
8x DDR4 Memory Channels per CPU
80x Gen4 PCIe Lanes (industry leading)
16x OpenCAPI Lanes (25Gbps)
48 V2 Open Rack compatible
OpenPOWER Boot Firmware
OpenBMC
Zaius deployed in Google’s Data Center
Rethink the Data Center