Acceleration Opportunities with CAPI

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Acceleration with CAPI

- CAPI provides the opportunity to create a wide range of acceleration solutions.
- Key benefits include both performance and ease of programming relative to I/O attached accelerators.
  - Closer coupling of accelerator (AFU):
    - Better throughput
    - Less overhead of data transfers
  - Coherent attach allows sharing of memory buffers:
    - Easier porting of programs targeted at standard CPU
    - Easier program development
    - Easier debug
Acceleration in CAPI system

- Acceleration Function
  - Data or Compute Intensive, Storage or External I/O. Can be developed with RTL or OpenCL

- Application Portion:
  - Data Set-up, Control

- Sharing the same memory space
  - Accelerator is a peer to POWER8 Core

- POWER8 Processor

CAPI Developer Kit Card
CAPI vs. I/O Device Driver: Data Prep

Typical I/O Model Flow:

- **DD Call**
  - 300 Instructions
  - 7.9µs

- **Copy or Pin Source Data**
  - 10,000 Instructions

- **MMIO Notify Accelerator**

- **Acceleration**
  - Application Dependent, but Equal to below

- **Poll / Interrupt Completion**

- **Copy or Unpin Result Data**
  - 3,000 Instructions

- **Ret. From DD Completion**
  - 1,000 Instructions

  **Total ~13µs for data prep**

Flow with a Coherent Model:

- **Shared Mem. Notify Accelerator**
  - 400 Instructions

- **Acceleration**
  - Application Dependent, but Equal to above

- **Shared Memory Completion**
  - 100 Instructions

  **Total 0.36µs**

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OpenPOWER™
I/O based memory sharing

Source: Intel and Khronos Group
Coherent Memory Sharing

Source: Intel and Khronos Group
Nallatech’s 385 card is the first supported CAPI FPGA accelerator card.

Nallatech, IBM and Altera have collaborated to provide the OpenPOWER CAPI Developer Kit for POWER8, which includes everything needed to start developing with CAPI in a POWER8 System.

Nallatech is also working with select partners and OpenPOWER members on custom hardware and CAPI enabled solutions.

### Nallatech’s CAPI Developer Kit Contents

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<tr>
<th>Included in CAPI Developer Kit</th>
<th>Hardware Components</th>
<th>Software / IP Components</th>
<th>Tools</th>
<th>Documentation</th>
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<tr>
<td>Nallatech 385 FPGA Accelerator</td>
<td>IBM CAPI Power Service Layer (PSL) (Encrypted FPGA IP)</td>
<td>Altera Quartus FPGA Tools</td>
<td>White Paper and Decision Guide</td>
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<tr>
<td>Nallatech JTAG Debug Kit</td>
<td>CAPI Host Support Library (libcxl)</td>
<td>PSL Simulation Engine</td>
<td>CAPI User's Guide</td>
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<td>'Memcopy' Example</td>
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<td>385 FPGA Card User Guide</td>
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<tr>
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<tr>
<td>Power 8 System (IBM Model 8247-21L or 8247-22L)</td>
<td>CAPI Enabled O/S (initially Ubuntu 14.10 LE from Canonical)</td>
<td>HDL Simulator (i.e. Cadence, Mentor, Synopsis)</td>
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Nallatech 385 FPGA Accelerator

Low cost, low power, high performance

- Half height, half length PCIe form factor (NIC-size)
- Altera Stratix V FPGA: D5 or A7
- PCIe Gen3x8 or CAPI host interface: Up to 10GBytes/sec sustained bandwidth
- (2) SFP+ network ports supporting multiple standards and speeds
- (2) banks of DDR3 SDRAM: up to 16GB total
OpenCL development for CAPI

Complete software only development environment for FPGA

main() {
    read_data( ... );
    manipulate( ... );
    clEnqueueWriteBuffer( ... );
    clEnqueueNDRange(...,sum,...);
    clEnqueueReadBuffer( ... );
    display_result( ... );
}

__kernel void sum
(__global float *a,
__global float *b,
__global float *y)
{
    int gid = get_global_id(0);
    y[gid] = a[gid] + b[gid];
}

Supports OpenCL 2.0 compatible share virtual memory feature
How Do I Get Started?

Contact Nallatech today for additional information or to request a quote for the CAPI Developer Kit.

We are happy to discuss how your specific application can benefit by leveraging CAPI solution.

You can also learn more about CAPI at:

nallatech.com/capi

Learn More About CAPI

Take a Deeper Technical Dive
Thank You

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